PATENT SPECIFICATION 1,161,206

DRAWINGS ATTACHED.

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COMPLETE SPECIFICATION.

Improvements relating to Frequency Synthesisers.

We, THE PLESSEY COMPANY LIMITED, a British Company of 56 Vicarage Lane, Ilford, Essex, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to frequency synthesisers.

More specifically, the invention relates to frequency synthesisers of the digital type in which the output frequency of a variable oscillator is controlled in accordance with the setting of a variable divider which divides the output frequency of the oscillator to produce a frequency which is compared with a comparison frequency derived from a standard or reference frequency oscillator, which frequencies are identical when the variable oscillator is producing the desired output frequency but which differ from each other in the event that the oscillator frequency departs from such desired frequency, the frequency difference being detected in order to afford an error signal which is utilised for correcting the variable oscillator output.

The output frequency from the variable oscillator is selectable by appropriate setting of the variable divider. Conventionally, the minimum frequency increments provided by the variable divider are at least equal to the comparison frequency (typically 1 kc) and the bandwidth of the usual phase error control loop of the synthesiser is therefore considerably less than the incremental adjustments in frequency afforded by adjustment of the variable divider. Consequently, to achieve small increments in frequency adjustment a very narrow bandwidth is required to be used. This has the disadvantage of preventing rapid changing of the variable divider settings and reduces the effectiveness of the phase loop control in attenuating unwanted frequency modulation.

According to the present invention a frequency synthesiser of the type hereinbefore described includes a frequency changing arrangement interposed between the output of the variable oscillator or that of a fixed divider driven therefrom and the variable divider, the frequency changing arrangement comprising a circuit arrangement for providing quadrature components of the oscillator output frequency or sub multiple thereof and respective modulators for modulating these quadrature components with the quadrature components of a modulating frequency which is low compared with the modulated frequency and the outputs of the modulators being combined to provide a single side band which is fed to the variable divider.

Thus by varying the modulation frequency continuous tuning of the variable oscillator is provided for.

For the purpose of producing the quadrature component of a subharmonic of the oscillator output a so-called double rank binary divider may be employed which is arranged to receive input signals displaced by 180° and which effects a division-by-two of the oscillator frequency whilst affording the requisite 90° shift between outputs of the binary divider without the need for filters.

The modulating frequency will be obtained from a modulating oscillator whose output is fed on the one hand direct to one of the modulators and on the other hand through a 90° phase shift network to the other modulator.

By means of the synthesiser according to the present invention continuous tuning of the

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variable oscillator can be provided by adjustment of the modulating frequency.

By way of example the invention will now be described with reference to the block schematic drawing of a digital synthesiser accompanying the Provisional Specification.

Referring to the drawing, the synthesiser illustrated comprises a variable or slave oscillator 1 the output from which is applied to buffer amplifier 2. The output from the amplifier 2 is passed to a phase splitter 3 providing two signals displaced by 180°. The phase splitter 3 has its outputs connected to the respective input gates of master-slave bistable circuits of a double-rank binary divider circuit 4 which divides the frequency of the input signals by two and affords two outputs in quadrature.

The quadrature outputs from the double-rank binary divider 4 are applied respectively as switching signals to the inputs of balanced modulators 5 and 6 to which modulating frequency signals derived from a modulating oscillator 7 are fed direct and via a 90° phase shift circuit 8. The outputs from the modulators 5 and 6 are combined to afford a single sideband signal which is passed through high frequency low-pass filter 9 which filters out high frequency spurious components near harmonics of the desired output frequency. This filter will need to be "band-switched" if the synthesiser is to cover a wide frequency of operation. The output from the low-pass filter is applied to a digital variable divider 10 which may in accordance with common practice comprise a number of cascaded digital counters. The divided output from the variable divider 10 is fed to a phase comparator 11 which also receives a comparison frequency derived from a reference (e.g. crystal) oscillator 12 via fixed divider 13. Any difference in phase between the comparison frequency and the frequency output from the variable divider is detected by the phase comparator 11 which accordingly provides an output signal filtered by a low frequency low-pass filter 14 before being applied to some means associated with the variable oscillator 1 for the adjustment of the variable oscillator output frequency to reduce the phase difference referred to above to zero.

The components contained within the dashed box in the drawing serve to divide the output frequency of the variable oscillator by two and to add to or subtract from such divided frequency the modulating frequency.

$$\text{Thus } Fv = \frac{Fo}{2} \pm Fm$$

Where; Fv is the frequency applied to the variable divider;

Fo is the variable oscillator output frequency; and

Fm is the modulating frequency.

Addition or subtraction of the modulating frequency (Fm) may be selected by appropriately arranging the 90° phase shifts.

In the steady state of the synthesiser when the output frequency from the variable oscillator is the desired frequency.

$$Fo = 2\,(Fv \mp Fm) = 2\,(NFc \mp Fm)$$

Where; Fc is the comparison frequency; and

N is the variable divider ratio (any positive integer).

Thus if frequency Fm is made variable over a range not less than Fc the output frequency of the oscillator may be set to any desired value.

Because of the narrow bandwidth of the phase control loop the signal fed to the variable divider 10 does not need to be very pure in order to obtain an output of acceptable purity from the slave oscillator 1. For instance, if frequency Fc is 500 c/s and the so-called "loop catching range" is 6%, no more than 1c/s peak deviation of the variable oscillator output frequency can be caused by a spurious component at the variable divider input which is 20 dB below the wanted signal. It is not difficult to achieve this order or purity of the signal feeding the variable divider with the arrangement just above described.

As will be appreciated from the foregoing description of one embodiment, the invention enables continuous tuning of the variable oscillator to be achieved by variation of the modulating frequency and moreover a relatively poor single sideband generator may be used.

The present invention may advantageously be applied to a general purpose communications receiver which may be required to follow a drifting transmission by manual or automatic operation as well as requiring the facility to be tuned to within 50 C/s, say, of arbitrary frequency in order to receive a single sideband transmission.

Attention is directed to our co-pending patent application number 41305/65 (Serial No. 1,161,205) which also relates to frequency synthesis.

WHAT WE CLAIM IS:—

1. A frequency synthesiser of the type hereinbefore defined, including a frequency changing arrangement interposed between the output of the variable oscillator or a fixed divider driven therefrom and the variable divider, the frequency changing arrangement comprising a circuit arrangement for providing quadrature components of the oscillator output frequency or a sub multiple thereof, as the case may be, and respective modulators for modulating these quadrature components with the quadrature components of a modulating frequency which is low

compared with the modulated frequency and the outputs of the modulators being combined to provide a single side band which is fed to the variable divider.

2. A frequency synthesiser as claimed in claim 1, in which the quadrature components of a sub-harmonic of the oscillator output are produced by a double rank binary divider which is arranged to receive input signals displaced by 180° from a phase splitter arrangement and which effects a division-by-two of the oscillator frequency whilst affording the requisite 90° shift between outputs of the binary divider.

3. A frequency synthesiser substantially as herein described with reference to the drawing accompanying the Provisional Specification.

4. A communications receiver continuously tuned by a frequency synthesiser as claimed in any preceding claim.

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For the Applicants.

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